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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,087	01/14/2004	Arup Bhattacharyya	MI22-2473	2443

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,087	BHATTACHARYYA, ARUP	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/14/02 - 7/8/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *71-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *71-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14, 4/21, 7/8/4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application on 1/14/04.

Information Disclosure Statement

1. The examiner acknowledges receipt of Information Disclosure Statements (IDS) filed 1/14/04, 4/21/04 and 7/8/04. The following items in the IDS filed 1/14/04 are only available in incompletely readable form: AC, AD, AF, AH, AJ, AQ, BC, BG and BH. Therefore, the IDS filed 01/14/04 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

2. Signed copies of the IDS Forms PTO-1449 have been enclosed with this office action, but above-listed incompletely readable items in IDS of 1/14/04 have been crossed out. The Information Disclosure Statements filed 4/21/04 and 7/8/04 have been considered.

Claim Objections

3. ***Claim 71*** is objected to because of the following informalities: the wording: "an entirety of the first active region within the crystalline layer being within" (lines 10-11) should be replaced by: "said portion being entirely within". Appropriate correction is required.

4. ***Claim 77*** is objected to because of the following informalities: the wording: "the transistor device" (line 1) should be replaced by: "the first transistor device". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. ***Claim 71-78 and 80-81*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu et al (6,251,751 B1) in view of Meyerson et al (5,298,452). Chu et al teach (title, abstract, Figure 6; cols. 2-5): a computer system (N.B.: as shown below an inverter, which is a computer system by itself, although other applications, including incorporation into a computer circuit, in particular DRAM, is also taught by Chu et al: see col. 5, l. 23-34) comprising:

a signal source arranged to provide a data signal (input: col. 4, l. 59-64); and an inverter coupled with the signal source (N.B.: inherently, a CMOS circuit of two (n-type and p-type, resp.) FETs (col. 4, l. 55-57) with gates interconnected to the same voltage source (input) (col. 4, l. 59-64) and the drain of one FET coupled to the source of the other (col. 4, l. 59-64) is an inverter circuit; see, e.g., any text book or specification, [0012]) coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; a crystalline layer comprising silicon and germanium 16' (col. 2, l. 27-29 and col. 3, l. 11-16); a first transistor device 52 (or, in an alternative

mode of identification: 53; col. 4, l. 32) supported by the crystalline layer (Fig. 6), the first transistor device comprising a first gate 57 (col. 4, l. 37-40) and a first active region (region laterally defined in view of the specification to comprise all of source and drain regions 60 and 61 (col. 4, l. 40-43) and semiconductor region contiguous with said source an drain regions) proximate the first gate (cf. Figure 6); the first active region including a first channel region (semiconductor region defined as being laterally between the source and drain regions 60 and 61) and a pair of first source/drain regions 60 and 61, respectively (loc.cit.); at least a portion of the first active region being within the crystalline layer (namely: the portion of the silicon germanium layer 16' located laterally between said source and drain regions 60 and 61, respectively); a second transistor device 53 (or 52) (Figure 6 and col. 4, l. 32), the second transistor device comprising a second gate 57and a pair of second source/drain regions 60 and 61 (cf. Figure 6; col. 4, l. 32-44); the first and second gates being electrically connected to one another (cf. Fig. 6 and col. 4, l. 59-64), and being in electrical connection with the signal source (namely: the input: col. 4, l. 64); and one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output (col. 4, l. 59-64 and Fig. 6).

Chu et al do not necessarily teach the limitation "an entirety of the first active region within the crystalline layer being within a single crystal of the crystalline layer" (lines 10-11 of claim 71). *However, it would have been obvious to include said limitation in view of Meyerson (5,298,452) cited by Chu et al for the process of making said crystalline layer 16' (see Chu et al, col. 2, l. 45-50), because Meyerson*, in a patent on

the chemical vapor deposition of epitaxial layers (title), hence analogous art, teach the epitaxial layer deposition to result in a single crystal (abstract and col. 19, l. 11-14). *Motivation* to include the teaching by Meyerson in the invention by Chu et al is assured because there is no reason to deviate from the method by Meyerson and recited for the step of producing the crystalline layer by Chu et al themselves (col. 2, l. 45-50). *Additional motivation* derives from the reduction of defects by virtue of the single-crystal nature of the product by Meyerson: crystal defects reduce mobility and hence lead to a deterioration of the electrical properties of the epitaxial layer (col. 3, l. 18-25).

On claim 72: the crystalline layer has a relaxed crystalline lattice (col. 2, l. 45-50), and further comprising a strained crystalline lattice layer 20' (see Chu et al, claim 10 and its independent claim 1; col. 5, l 38-48 and col. 6, l. 21-23) between the crystalline layer and 16' and the first transistor device gate 57.

On claim 73: the strained crystalline layer includes silicon (col. 2, l. 51-57).

On claim 74: the first transistor device 52 is an NFET device (col. 4, l. 55-56).

On claim 75: in the alternative indicated in the rejection of claim 71 the first transistor device is a PFET device (loc. cit.).

On claim 76: the strained crystalline lattice 16' layer includes silicon and germanium (col. 2, l. 51-57).

On claim 77: in the alternative indicated in the rejection of claim 71 the first transistor device is a PFET device (loc. cit.).

On claim 78: in the combined invention, Chu et al follows the method by Meyerson, thus producing the entirety of the relaxed crystalline lattice 16' as a single

crystal (Chu et al, col. 2, l. 45-57 and Meyerson, abstract, first sentence, and claim 13 by Meyerson).

On claim 80: the relaxed crystalline lattice 16' includes Si/Ge (col. 2, l. 51-57).

On claim 81: the relaxed crystalline lattice comprises from 15 - 25 atomic percent germanium (col. 2, l. 35-37), and hence the range of atomic percent germanium in the prior art by Chu et al is seen to overlap the range as claimed.

A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). In the underlying case there is substantial overlap and obviousness is thus fully *prima facie*.

7. ***Claims 71, 72 and 79*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fitzgerald et al (US 2002/0125471 A1) in view of Chu et al (6,251,751 B1) and Meyerson (5,298,452). Fitzgerald teaches a computer system (CMOS inverter circuit is a computer system) comprising: a signal source (input node 401 (Fig. 4A and [0064]) arranged to provide a data signal V_{in} (Fig. 4A and [0064]); and an inverter 400 coupled with the signal source (Fig. 4A and [0064]), configured to invert the data signal ([0064]) and arranged to output the inverted signal (through output node 410 (Fig. 4A and [0064]); the inverter including: a crystalline layer 502/506 (Figure 5A and [0084]: layer 502/506 is characterized by lattice constants, including partly relaxed (i.e., buffer) layer 502 and therefore it must have crystallinity (see [0055], first sentence):

106 and 506 denote the same layer, so do 102 and 502) comprising silicon and germanium ([0054] and [0084]); a first transistor device (either nMOSFET or pMOSFET, see abstract) supported by the crystalline layer, the first transistor device comprising a first gate 512 ([0084]) and a first active region (defined in view of the specification to comprise all of the semiconductor region laterally confined between and inclusive of source and drain regions 563 and 564, respectively ([0087] and Figure 5A) proximate the first gate (Fig. 5A); the first active region including a first channel region (active region portion between source and drain) and a pair of source and drain regions 563 and 564, respectively ([0087]); at least a portion of the first active region being within the crystalline layer (the portion between source and drain 506 being within 504/502/506; [0084]); a second transistor device (the other of the nMOSFET and pMOSFET delineated above and not identified to be said first transistor device) comprising a second gate and a pair of second source and drain regions ([0084]); the first and second gates being electrically connected to one another and being connected to a signal source (401, V_{in})(Figure 4A and [0064];the gates being interconnected and connected to an input signal source also is inherent in a CMOS inverter); and one of the first source/drain regions being electrically connected with one of the second source/drain regions (inherent in any CMOS inverter and shown in Fig. 4A) and being in electrical connection with the output 410 (Fig. 4A and [0064]). Fitzgerald et al do not necessarily teach the limitation "an entirety of the first active region within the crystalline layer being within a single crystal of the crystalline layer". However, it would have been obvious to include said limitation in view of Chu et al, who teach the deposition of an

epitaxial crystalline silicon germanium layer 16' as a relaxed silicon germanium crystalline layer in a CMOS inverter heterostructure (col. 1, l. 45-62), with reference to Meyerson for the deposition method (col. 2, l. 23-50 and Figure 1) of said layer. Material result and *motivation* are recited in Meyerson: his method results in a single crystal silicon germanium layer.(see abstract) while for motivation Meyerson cites the reduction of defects by virtue of the single-crystal nature of the product by Meyerson: crystal defects reduce mobility and hence lead to a deterioration of the electrical properties of the epitaxial layer (Meyerson, col. 3, l. 18-25).

On claim 72: the crystalline layer 502/506 has a relaxed crystalline lattice (abstract, [0055] and [0084]) while the computer system further comprises a strained crystalline layer 508 (see [0084]: in order a layer to be strained, i.e., to have a strained lattice, a lattice must exist and hence the layer is crystalline.

On claim 79: lattice mismatch is spread over a distance by silicon germanium buffer layer 502, which buffer layer, being by its gradual accommodation of lattice constant at least partly relaxed. Therefore, some of the mismatch must reside in 502/506 including the interface between 502 and 506. Any lattice mismatch implies at least two different lattice constant values and hence two different lattices and related crystals. Therefore, the relaxed crystalline lattice in 502/506 is polycrystalline.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
September 7, 2005

Patent Examiner:

Johannes Mondt (art Unit: 2826).